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National Semiconductor

May 2002

LM1269
110 MHz I²C Compatible RGB Video Amplifier System with OSD & DACs

General Description

The LM1269 pre-amp is an integrated CMOS CRT pre-amp. The IC is I²C compatible, and allows control of all the parameters necessary to directly setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs, and is well matched to the LM2479 and LM2480 integrated bias clamp IC.

The LM1269 pre-amp is designed to work in cooperation with the LM246X high gain driver family.

Black level clamping of the signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional black level clamp capacitors.

The IC is packaged in an industry standard 24-lead DIP molded plastic package.

Features

- I²C compatible interface
- 110 MHz bandwidth preamplifier with full video signal parametric control
- 4 external 8-bit DACs for bus controlled Bias and Brightness
- Suitable for use with discrete or integrated clamp, with software configurable Brightness mixer
- Power Save (Green) Mode, 80% power reduction
- Matched to LM246X driver

Applications

- Low end 14', 15', and 17' bus controlled monitors with OSD
- 1024 X 768 displays up to 70 Hz requiring OSD capability
- Very low cost system with LM246X driver

Block and Connection Diagram

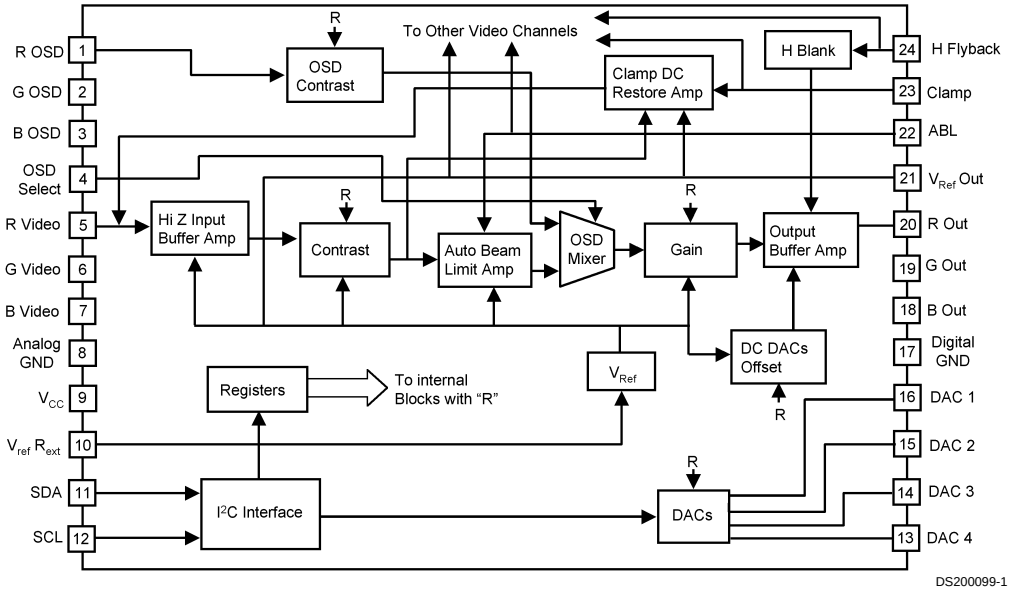

FIGURE 1. Order Number LM1269NA
See NS Package Number N24D

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Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, Pin 9	6.0V
Peak Video Output Source Current (Any One Amp) Pins 18, 19, or 20	28 mA
Voltage at Any Input Pin (V_{IN})	V_{CC} +0.5 > V_{IN} > −0.5V
Power Dissipation (P_D) (Above 25˚C Derate based on θ_{JA} and T_J)	2.4W
Thermal Resistance to Ambient (θ_{JA})	51˚C/W
Thermal Resistance to Case (θ_{JC})	32˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 4)	3.5 kV
ESD Machine Model (Note 5)	350V
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	265˚C

Operating Ratings (Note 2)

Temperature Range	0˚C to 70˚C
Supply Voltage (V_{CC})	4.75V < V_{CC} < 5.25V
Video Inputs	0.0V < V_{IN} < 1.0V_{P-P}

Active Video Signal Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Output = 2 V_{P-P}.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
I_S	Maximum Supply Current	Test Setting 1, R_L = ∞ (Note 8)		200	225	mA
I_{S-PS}	Maximum Supply Current, Power Save Mode	Test Setting 1, R_L = ∞, Bit 1 of Reg. 9 = 1 (Note 8)		42	60	mA
LE	Linearity Error	Test Setting 4, Triangular signal input source (Note 9)		5		%
$V_{O\ Blk\ Typ}$	Typical Video Black Level Output	Test Setting 4, No AC Input Signal, DC = 5 Hex, or 0.5V Offset	1.05	1.25	1.45	VDC
$V_{O\ Blk\ Step}$	Video Black Level Step Size	Test Setting 4, No AC Input Signal	60	90	120	mV
$\Delta V_O/\Delta V_{CC}$	Variation in Output Video Black Level vs V_{CC} Variations	Test Setting 1 & 3, No AC Input Signal, 4.75<V_{CC}<5.25	−0.25	0	0.25	mV/V
$V_{O\ White-Max}$	White Level Video Output Voltage	Test Setting 3, Video in = 0.7V	4.0	4.2		V
V_{Blank}	Blanked Output Level	Test Setting 4, AC Input Signal	0	0.2	0.5	V
t_r	Rise Time	10% to 90%, Test Setting 4, AC Input Signal (Note 10)		3.9		ns
OS_R	Overshoot (Rising Edge)	Test Setting 4, AC Input Signal (Note 10)		1		%
t_f	Fall Time	90% to 10%, Test Setting 4, AC Input Signal (Note 10)		3.5		ns
OS_F	Overshoot (Falling Edge)	Test Setting 4, AC Input Signal (Note 10)		1		%
f(−3 dB)	Video Amplifier Bandwidth (Note 13)	Test Setting 8		110		MHz
V_{sep} 10 kHz	Video Amplifier 10 kHz Isolation	Test Setting 8 (Note 14)		−70		dB
V_{sep} 10 MHz	Video Amplifier 10 MHz Isolation	Test Setting 8 (Note 14)		−50		dB
$A_{V\ Max}$	Maximum Voltage Gain	Test Setting 8, AC Input Signal		4		V/V
$A_{V\ ½}$	Contrast @ 50% Level	Test Setting 5, AC Input Signal		−10		dB
$A_{V\ Min}$	Maximum Contrast Attenuation	Test Setting 2, AC Input Signal		−20		dB
$A_{V\ Gain\ ½}$	Gain @ 50% Level	Test Setting 6, AC Input Signal		−5		dB
$A_{V\ Gain\ Min}$	Maximum Gain Attenuation	Test Setting 7, AC Input Signal		−10		dB
$A_{V\ Match}$	Absolute Gain Match @ $A_{V\ Max}$	Test Setting 3, AC Input Signal		±0.5		dB

Active Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Output = 2 V_{P-P}.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
$A_{V\ Track}$	Gain Change between Amplifiers	Tracking when Changing from Test Setting 8 to Test Setting 5 (Note 11)		±0.5		dB
$V_{ABL\ TH}$	ABL Control Upper Limit	Test Setting 4, AC Input Signal (Note 12)		5		V
$V_{ABL\ Range}$	ABL Control Voltage Active Range	Test Setting 4, AC Input Signal (Note 12)		2		V
ΔA_{ABL}	ABL Control Range	Test Setting 4, AC Input Signal (Note 12)		−8		dB
$I_{ABL\ Active}$	ABL Input Bias Current during ABL	Test Setting 4, AC Input Signal, V_{ABL} = 2V(Note 12)		0	10	µA
$I_{ABL\ Max}$	ABL Input Current Clamp Sink Capability	Test Setting 4, AC Input Signal (Note 12)			1	mA
$V_{Clamp\ Max}$	Clamp Gate Low Input Voltage	Clamp Comparators Off			1.4	V
$V_{Clamp\ Min}$	Clamp Gate High Input Voltage	Clamp Comparators On	2.6			V
I_{Clamp}	Clamp Gate Input Current	V_{23} = 0V to V_{CC} − 1V	−5	0.1	10	µA
$t_{PW\ Clamp}$	Back Porch Clamp Pulse Width	(Note 15)	200			ns
$t_{Clamp\text{-}Video}$	End of Clamp Pulse to Start of Active Video	Limit is guaranteed by design	200			nsec
$R_{In\text{-}Video}$	Input Resistance	Test Setting (4)		20		MΩ
$I_{In\text{-}Video}$	Input Bias Current	Test Setting (4)		0.1	10	µA
V_{Ref}Out	V_{Ref} Output Voltage	10 kΩ, 1% Resistor; Pin 10 to GND	1.25	1.40	1.55	V
V_{Spot}	Spot Killer Voltage	V_{CC} Adjusted to Activate	3.6	4.0	4.25	V

OSD Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Signal Output = 2 V_{P-P}, Test Setting 8.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
$V_{OSD\text{-}L}$	OSD Input Low Input Operating Range	OSD Inputs are Selected			1.2	V
$V_{OSD\text{-}H}$	OSD Input High Input Operating Range	OSD Inputs are Selected	2.5			V
I_{OSD}	OSD Input Current	V_{OSD} = 0V to V_{CC} − 1V	−5	0.1	10.0	µA
$V_{OSD\text{-}Sel\text{-}L}$	OSD Select Low Input Operating Range	Video Inputs are Selected			1.2	V
$V_{OSD\text{-}Sel\text{-}H}$	OSD Select High Input Operating Range	OSD Inputs are Selected	2.5			V
$I_{OSD\text{-}Sel}$	OSD Select Input Current	$V_{OSD\text{-}Sel}$ = 0V to V_{CC} − 1V	−5	0.1	10	µA
$\Delta V_{O\text{-}OSD(Blk)}$	OSD ΔBlack Level Output Voltage, Difference from Video Output	Register 08 = 18, Minimum Video Black Level		±45	±150	mV
$V_{O\text{-}OSD(Blk)}$	Range of OSD Black Level Output Voltage between the 3 Channels	Register 08 = 18, Minimum Video Black Level	−100	0	+100	mV
$V_{OSD\text{-}out}$	OSD Output Voltage, Percent of Maximum Video Out	Register 08 = 18, Minimum Video Black Level	75	88	100	%
$\Delta V_{OSD\text{-}out}$	OSD Output V_{P-P} Attenuation	Register 08 = 08	58	63	68	%
$V_{OSD\text{-}out}$ (Track)	Output Variation between Channels	Register 08 Changed from 18 to 08		±3.0	±5.0	%

OSD Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Signal Output = 2 V_{P-P}, Test Setting 8.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
$\Delta t_{OSD/OSD\ S}$	Output Skew Time between OSD and OSD Select	Measured from 50% Point on all Waveforms		±2.0		ns
V_{feed} 10 kHz	Video Feedthrough into OSD	OSD Inputs = 0V		−70		dB
V_{feed} 10 MHz	Video Feedthrough into OSD	OSD Inputs = 0V		−60		dB

External DAC Signals Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Signal Output = 2 V_{P-P}. The following apply for all four external DACs.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
$V_{Min\ DAC}$	Min DAC Output Voltage	Value = 00h		0.5	0.75	V
$V_{Max\ DAC}$ Mode 00	Max DAC Output Voltage	Value = FFh, DCF[1:0] = 00h (no load)	3.6	4.2		V
$V_{Max\ DAC}$ Mode 11	Max Output Voltage of DACs 1–3 in DCF Mode 11	Value = FFh, DCF[1:0] = 11h, DAC4 Value = 00h	1.85	2.1	2.35	V
$\Delta V_{Max\ DAC}$ (Temp)	Variation of any DAC output voltage with temperature	0˚C<T<70˚C ambient		±0.5		mV/deg
$\Delta V_{Max\ DAC}$ (V_{CC})	Variation of any DAC output voltage with V_{CC}	4.75V<V_{CC}<5.25V		±50		mV/V
Linearity	Linearity of DAC Over its Range			5		%
Monotonicity	Monotonicity of the DAC	Excluding dead zones at limits of DAC		±0.5		LSB

External Interface Signals Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Output = 2 V_{P-P}.

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
$V_l(I^2C)$	I^2C Low Input Voltage	SDA or SCL Inputs	−0.5	0.5	1.5	V
$V_h(I^2C)$	I^2C High Input Voltage	SDA or SCL Inputs	3.0	4.0	5.0	V
$I_l(I^2C)$	I^2C Low Input Current	SDA or SCL Inputs, Input Voltage = 0V	1.9	2.2	2.5	µA
$I_h(I^2C)$	I^2C High Input Current	SDA or SCL Inputs, Input Voltage = 5V	0.3	0.6	0.9	µA
$t_{H\text{-}Blank\ on}$	H-Blank Time Delay from Zero Crossing Point of H Flyback	Rising Edge of the Flyback Signal		50		ns
$t_{H\text{-}Blank\ off}$	H-Blank Time Delay from Zero Crossing Point of H Flyback	Falling Edge of the Flyback Signal		50		ns
$I_{In\ Threshold}$	I_{In} H-Blank Detection Threshold			−20		µA
$I_{In\text{-}Operating}$	Minimum — Insure Normal Operation Maximum — Should Not Exceed in Normal Operation	Lowest Operating Horizontal Frequency in Given Application (Note 17)	−30		−300	µA
$I_{In\ Flyback}$	Peak Current during Flyback Period, Recommended Design Range	Operating Range for all Horizontal Scan Frequencies, Maximum Current Should Not Exceed 2 mA (Note 17)	0.5	1.5	2.0	mA

Note 1: Limits of Absolute Maximum Ratings indicate limits below which damage to the device must not occur.

Note 2: Limits of operating ratings indicate required boundaries of conditions for which the device is functional, but may not meet specific performance limits.

External Interface Signals Electrical Characteristics (Continued)

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Note 6: Typical specifications are specified at +25˚C and represent the most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The supply current specified is the quiescent current for V_{CC} with $R_L = \infty$. Load resistors are not required and are not used in the test circuit, therefore all the supply current is used by the pre-amp.

Note 9: Linearity Error is the variation in step height of a 16 step staircase input signal waveform with 0.7 V_{P-P} level at the input, subdivided into 16 equal steps, with each step approximately 100 ns in width.

Note 10: Input from signal generator: t_r, $t_f < 1$ ns. Scope and generator response used for testing: $t_r = 1.1$ ns, $t_f = 0.9$ ns. Using the RSS technique the scope and generator response have been removed from the output rise and fall times.

Note 11: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to A_V ½ and measured relative to the A_V max condition. For example, at A_V max the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to A_V ½. This yields a typical gain change of 10.0 dB with a tracking change of ±0.2 dB.

Note 12: ABL should provide smooth decrease in gain over the operational range of 0 dB to –6 dB

$$\Delta A_{ABL} = A(V_{ABL} = V_{ABL\ Max\ Gain}) - A(V_{ABL} = V_{ABL\ Min\ Gain})$$

Beyond –6 dB the gain characteristics, linearity, pulse response, and/or behavior may depart from normal values.

Note 13: Adjust input frequency from 10 MHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 14: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for $V_{sep\ 10\ MHz}$.

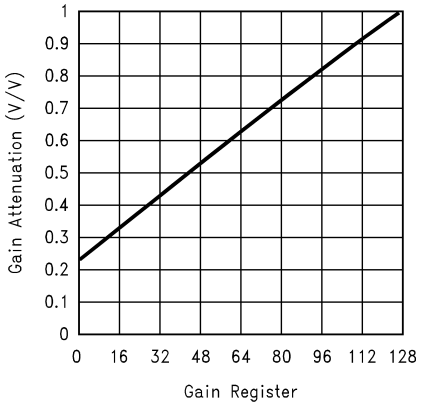
Note 15: A minimum pulse width of 200 ns is guaranteed for a horizontal line of 15 kHz. This limit is guaranteed by design. If a lower line rate is used then a longer clamp pulse may be required.

Note 16: The video black level is used for this test. OSD amplitude is measured from the video black level to the OSD white level.

Note 17: Limits met by matching the external resistor going to pin 24 to the H Flyback voltage.

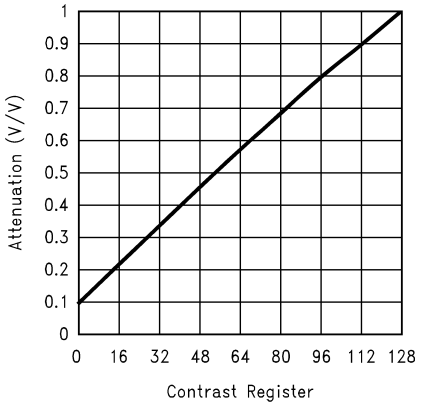
Typical Performance Characteristics V_{CC} = 5V, T_A = 25° unless otherwise specified.

Gain Attenuation



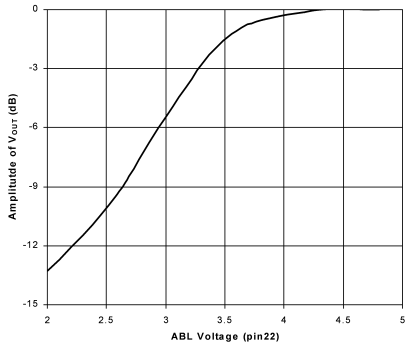
DS200099-2

Contrast Attenuation



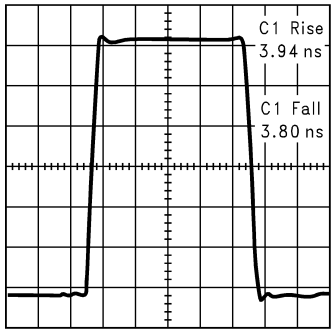
DS200099-3

ABL Attenuation



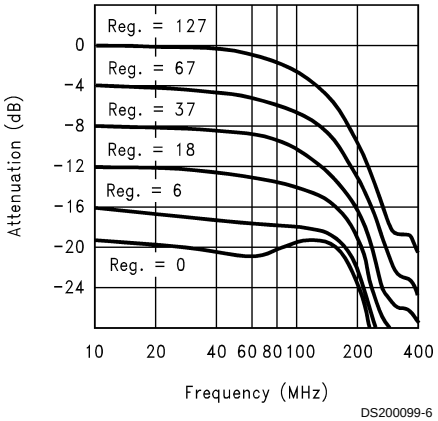
DS200099-4

Rise and Fall Times



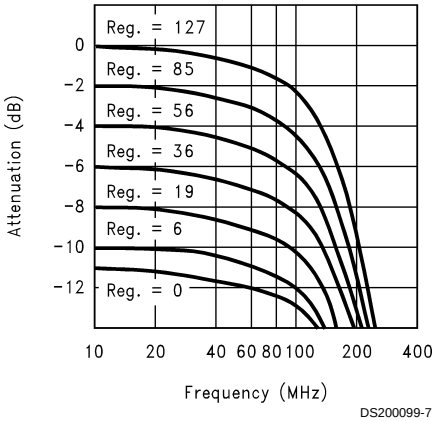
DS200099-5

Contrast vs Frequency



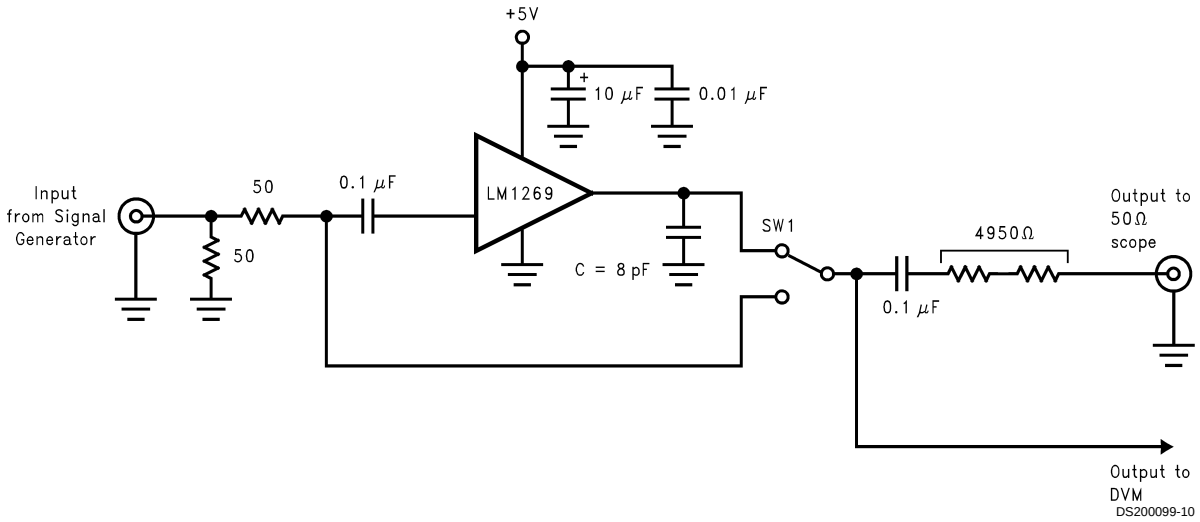
DS200099-6

Gain vs Frequency



DS200099-7

Test Circuit



Note: 8 pF load includes parasitic capacitance.

Test Settings

Control	No. of Bits	Basic Test Setting 1	Basic Test Setting 2	Basic Test Setting 3	Basic Test Setting 4	Basic Test Setting 5	Basic Test Setting 6	Basic Test Setting 7	Basic Test Setting 8
Contrast	7	Max (Hex 7F)	Min (Hex 00)	Max (Hex 7F)	Max (Hex 7F)	50% (Hex 40)	Max (Hex 7F)	Max (Hex 7F)	Max (Hex 7F)
R, G, B Gain	7	Max (Hex 7F)	Max (Hex 7F)	Max (Hex 7F)	Set Video Output to $2V_{P-P}$	Max (Hex 7F)	50% (Hex 40)	Min (Hex 00)	Max (Hex 7F)
Video DC Offset & OSD Contrast	5	Min (Hex 18)	Min + 0.5V (Hex 1D)	Max (Hex 07)	Min + 0.5V (Hex 1D)	Min + 0.5V (Hex 1D)	Min + 0.5V (Hex 1D)	Min + 0.5V (Hex 1D)	Min + 0.5V (Hex 1D)

Timing Diagrams

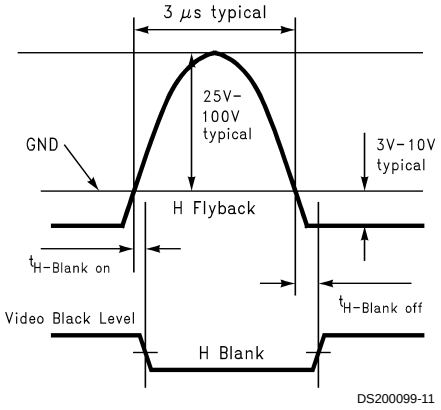
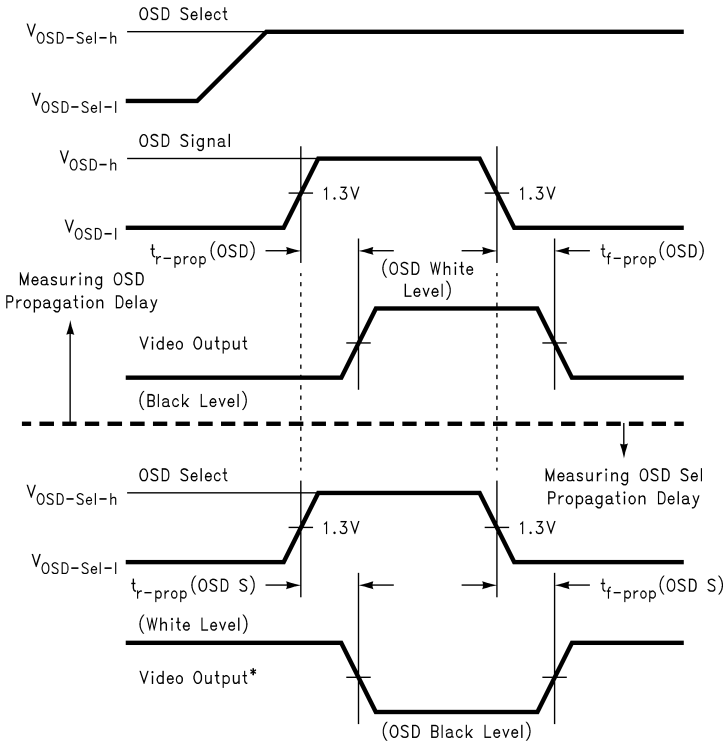


FIGURE 2. Blanking Propagation Delay

Timing Diagrams (Continued)



*OSD Signal (V_{OSD-l}) = black level and Video input = white level

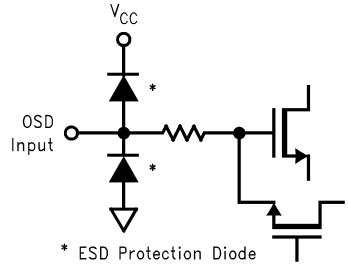
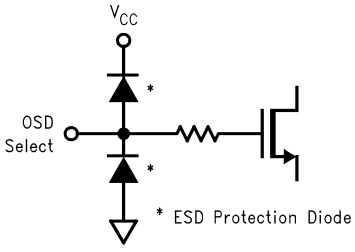
$\Delta t_{OSD/OSD\ S}$ **(OSD output skew) =** t_{r-prop}**(OSD) –** t_{r-prop}**(OSD S) and**

$\Delta t_{OSD/OSD\ S}$ **(OSD output skew) =** t_{f-prop}**(OSD) –** t_{f-prop}**(OSD S)**

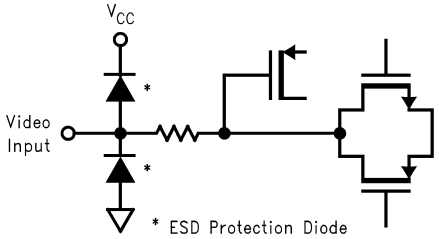
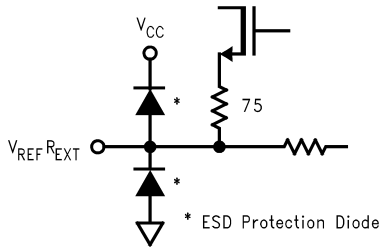
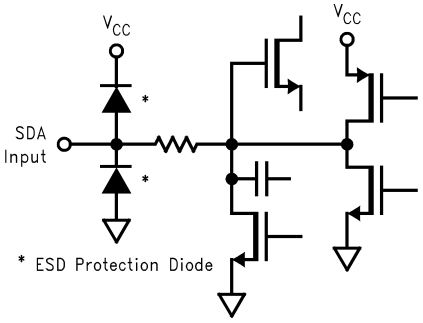
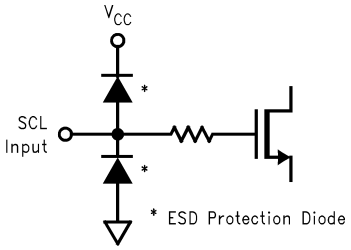
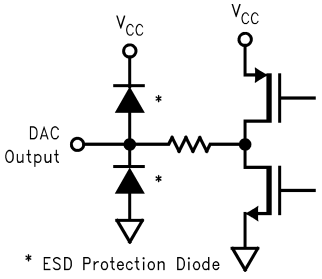
DS200099-12

FIGURE 3. OSD Output Skew

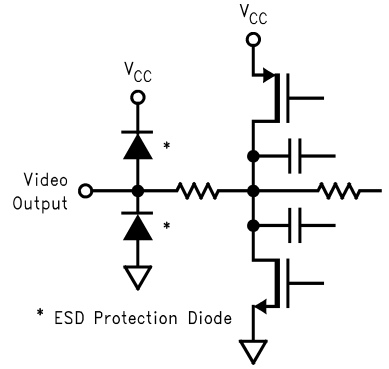
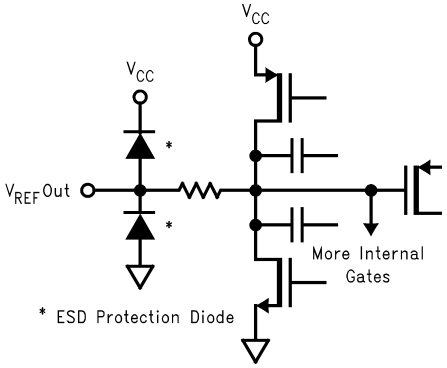
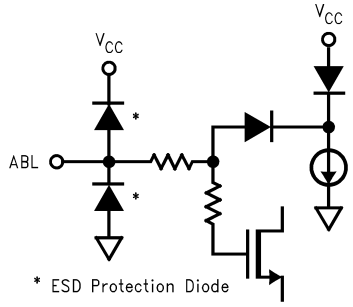
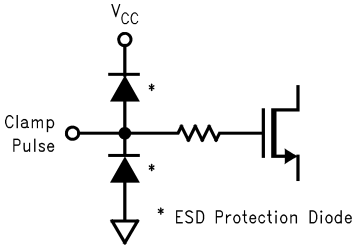
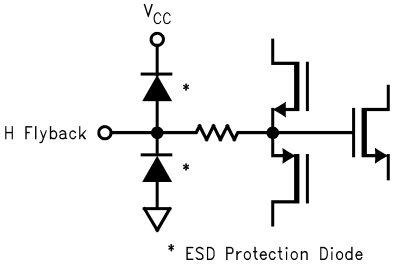
Pin Descriptions

Pin No.	Pin Name	Schematic	Description
1 2 3	Red OSD Input Green OSD Input Blue OSD Input		These inputs accept standard TTL or CMOS inputs. Each color is either fully on (logic high) or fully off (logic low). Unused pins should be connected to ground with a 47k resistor.
4	OSD Select		This input accepts a standard TTL or CMOS input. H = OSD L = Video Connect to ground with a 47k resistor if not using OSD.

Pin Descriptions (Continued)

Pin No.	Pin Name	Schematic	Description
5 6 7	Red Video In Green Video In Blue Video In		Video inputs. These inputs **must** be AC coupled with a 4.7 nF cap. DC restoration is done at these inputs. A series resistor of about 33Ω and external ESD protection diodes should also be used for ESD protection.
8	Analog Ground		Ground Pin for the analog circuits of the LM1269.
9	V_{CC}		Power supply pin for LM1269.
10	$V_{ref}R_{ext}$		Sets the internal current sources through a 10 kΩ 1% external resistor. Resistor value and accuracy is critical for optimum operation of the LM1269.
11	SDA		The I^2C data line. A pull-up resistor of about 2 kΩ should be connected between this pin and +5V. A 300Ω resistor should be connected in series with the data line for protection against arcing.
12	SCL		The I^2C Clock line. A pull-up resistor of about 2 kΩ should be connected between this pin and +5V. A 300Ω resistor should be connected in series with the clock line for protection against arcing.
13 14 15 16	DAC4 DAC3 DAC2 DAC1		DAC outputs for cathode cut-off adjustments and brightness control. DAC 4 can be set to change the outputs of the other three DACs, acting as the brightness control. The DACs are set through the I^2C bus.
17	Digital Ground		Ground Pin for the digital circuits of the LM1269.

Pin Descriptions (Continued)

Pin No.	Pin Name	Schematic	Description
18 19 20	Blue Video Out Green Video Out Red Video Out		Video outputs of the LM1269. The ideal driver for this part is the LM246X CRT driver family, which has the necessary gain of 26 dB or 20 V/V.
21	V_{Ref} Out		A 0.1 µF capacitor must be placed close to this pin for decoupling the internal V_{Ref}. This pin may be used for an external voltage reference with proper buffering.
22	ABL		The Auto Beam Limit control reduces the gain of the video amplifier in response to a control voltage proportional to the CRT beam current. The ABL acts identically on all three channels. ABL is required for CRT life and X-ray protection.
23	Clamp Pulse		This input accepts a standard TTL or CMOS input. A positive signal activates the clamp pulse for DC restoration of the video input. The AC coupling capacitors at the video inputs are used for holding the DC correction voltage, eliminating the need for additional capacitors.
24	H Flyback		H flyback is an analog signal input from the monitor horizontal scan. The LM1269 is able to generate an accurate blanking pulse in the video outputs from this input. The horizontal flyback from the monitor must be a clean signal, with no ringing or other noise on the signal.

Functional Description

All functions of the LM1269 are controlled through the I^2C Bus. Details on the internal registers are covered in the I^2C Interface Registers Section. *Figure 1* shows the block diagram of the LM1269. The I^2C signals come in on pins 11 and 12 and go to the I^2C Interface. Both the internal blocks with an "R" and the four external DACs are controlled by the I^2C Interface. The video and OSD blocks are shown for the red channel in *Figure 1*. The blocks for both the green and blue channels are not shown; however, they are identical to the red channel.

Proper operation of the LM1269 does require a very accurate reference voltage. This voltage is generated in the V_{Ref} block. To insure an accurate voltage over temperature, an external resistor is used to set the current in the V_{Ref} stage. The external resistor is connected to pin 10. This resistor should be 1% and have a temperature coefficient under 100 ppm/°C. ALL VIDEO SIGNALS MUST BE KEPT AWAY FROM PIN 10. This pin has a very high input impedance and will pick up any high frequency signals routed near it. The board layout shown in *Figure 10* is a good example of trace routing near pin 10. The output of the V_{Ref} stage goes to a number of blocks in the video section and also to pin 21. This pin allows capacitor filtering on the V_{Ref} output and offers an accurate external reference. A buffer must be used with this reference, the maximum current loading should be only 100 µA.

Note: Any noise injected into pin 21 will appear on the video. The voltage reference must be kept very clean for best performance of the LM1269.

The video inputs are pins 5, 6, and 7. Looking at the red channel (pin 5) note that the "Clamp DC Restore Amp" is connected to this pin. Since the video must be AC coupled to the LM1269, the coupling cap is also used to store the reference voltage for DC restoration. The "Clamp DC Restore Amp" block charges the input capacitor to the correct voltage when the clamp pulse (pin 23) is active. The "Hi Z Input Buffer Amp" buffers the video signal for internal processing. Input impedance to this stage is typically 20 MΩ. With such a high impedance the DC restoration can appear to be working for a number of minutes after the clamp pulse is removed.

The output of the Buffer Amp goes to the Contrast stage. The 7 bit contrast register (03h) sets the contrast level through the I^2C bus. This register controls the Contrast stage in each video channel. Contrast adjustment range is up to −20 dB. Loading all zeros in the contrast register gives −20 dB attenuation. All ones will give no attenuation. The output of this stage is used as the feedback for the DC restoration loop.

"Auto Beam Limit Amp" or ABL is the next block in the video path. This is a voltage controlled gain stage which gives no attenuation with 5V at pin 22 and gives about −10 dB attenuation with 2V at pin 2. ABL is covered in more detail later in this section.

Next in the video path is the "OSD Mixer". The OSD Select signal at pin 4 controls this stage, selecting OSD with a high at pin 4, and video with a low at pin 4. Since the DC restoration feedback is at the Contrast output, the video black level will match the OSD black level. The OSD signal is mixed with the video signal at the output of this stage.

The OSD goes through the "OSD Contrast" stage before entering the "OSD Mixer" block. Bits 3 and 4 of register 08h control the OSD contrast giving four video levels for the OSD window. Maximum video level for the OSD window occurs with both bits set to one. Minimum video level will occur with both bits set to a zero.

Following the "OSD Mixer" is the "Gain" block. Each video channel has its own independent control of this block so the user can balance the color of the CRT display. Registers 00h, 01h, 02h are used for the gain attenuation. These registers are 7 bits with the maximum attenuation of −10 dB occurring when all zeros are loaded.

The final block in the video path is the "Output Buffer Amp". This stage provides the drive needed for the inputs of a CRT driver. The recommended driver for this pre-amp is one of the LM246X family. Horizontal blanking is also added to the video signal from the "H Blank" stage. This block is covered in more detail below. DC offset of the output is set by the "DC DACs Offset" stage. Bits 0 through 2 in register 08 control this stage. This gives 8 different black levels ranging from 0.75V to 1.55V. When using one of the LM246X CRT driver family it is recommended that the black level be set to 1.25V.

ABL: The Auto Beam Limit control reduces the gain of the video amplifiers in response to a control voltage proportional to the CRT beam current. The ABL acts on all three channels in an identical manner. This is required for CRT life and X-ray protection. The beam current limit circuit application is as shown in *Figure 4:* when no current is being drawn by the EHT supply, current flows from the supply rail through the ABL resistor and into the ABL input of the IC. The IC clamps the input voltage to a low impedance voltage source (the 5V supply rail).

When current is drawn from the EHT supply, some of the current passing through the ABL resistor goes to the EHT supply, which reduces the current flowing into the ABL input of the IC.

When the EHT current is high enough, the current flowing into the ABL input of the IC drops to zero. This current level determines the ABL threshold and is given by:

$$I_{ABL} = \frac{V_S - V_{ABL\ TH}}{R_{ABL}}$$

Where:

V_S is the external supply (usually the CRT driver supply rail, about 80V)

$V_{ABL\ TH}$ is the threshold ABL voltage of the IC

R_{ABL} is the ABL resistor value

I_{ABL} is the ABL limit

When the voltage on the ABL input drops below the ABL threshold of the pre-amp, the gain of the pre-amp reduces, which reduces the beam current. A feedback loop is thus established which acts to prevent the average beam current exceeding I_{ABL}.

Functional Description (Continued)

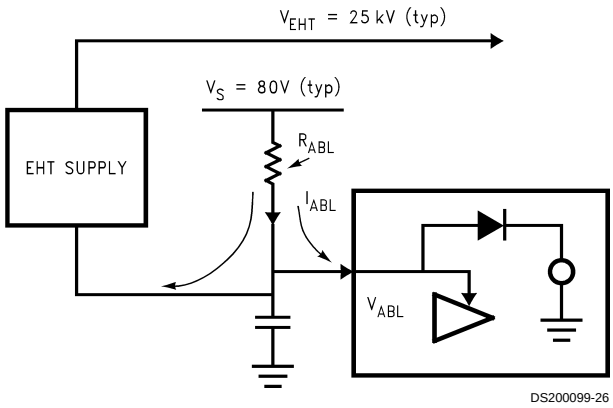


FIGURE 4. ABL

H Flyback: H Flyback is an analog signal input from the monitor horizontal scan. The "H Blank" section uses this signal to add horizontal blanking to the output video signal. This enables the user to blank at the cathodes during horizontal flyback. An optional capacitor and/or resistor to ground may be needed if noise interferes with the H Flyback signal.

This feature gives very accurate timing for the horizontal blanking; however, the flyback signal must be very clean. There should be no ringing or other noise on the flyback signal.

R_{LIMIT} is used to limit the input current into the IC to a typical value of + 1 mA during flyback and −100 µA during normal forward scan. For example if an H flyback with a peak of 100V is used, R_{LIMIT} = 100 kΩ. The internal input impedance of pin 24 is low to limit the maximum voltage swing at the input to within the supply rail and ground. The IC interface circuit creates a digital signal from this waveform, which is used as the blanking signal at the "Output Buffer Amp". This signal adds blanking to the video output signal. *Figure 5* shows the H flyback waveforms and the location of R_{LIMIT}. A 56 pF capacitor has been added to the H Flyback pin on the demo board for filtering noise on the H Flyback signal.

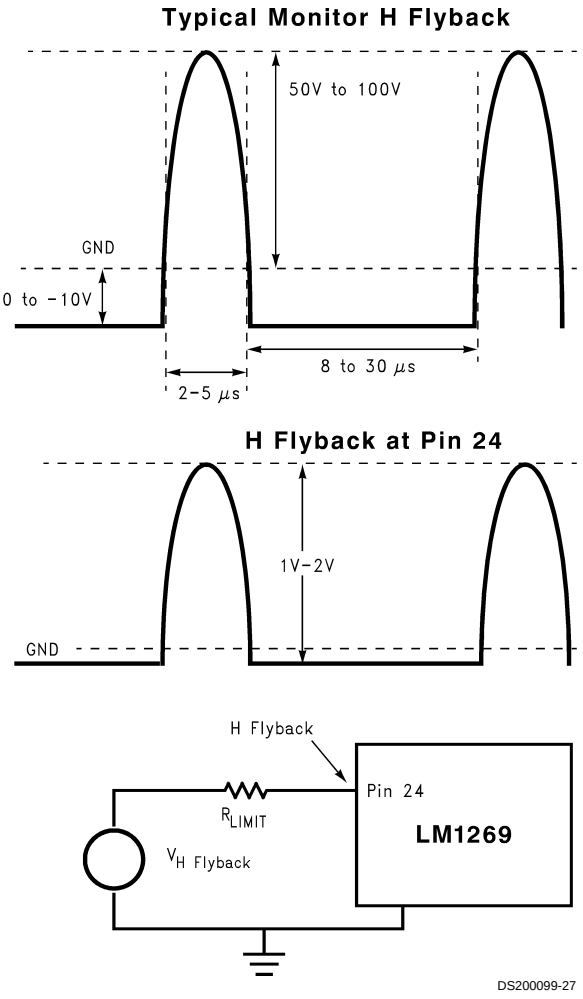


FIGURE 5. H Flyback Input Pulse

H Blank: Some customers may still prefer to use a standard logic signal for the horizontal blanking. Pin 24 can be adapted to accept a logic input. It is necessary for the current flow into pin 24 to reverse for proper operation. Therefore the logic signal must be AC coupled into pin 24. *Figure 6* shows the recommended circuit for a logic signal input. The blank signal must be a positive pulse.

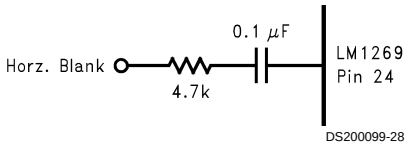


FIGURE 6. Standard Logic H Blank

Power Save Mode: There are two modes of power save:

1. Blanking the video
2. Turning off most of the power for maximum power savings.

In the first mode the video is completely blanked. By setting bit-0 in register 9 to a 1 the video will be completely blanked. This gives some power savings since there is no beam current in the monitor. Maximum power saving is obtained in the second mode. Bits 0 and 1 in register 9 should be set to a 1. Bit 1 in register 9 turns off the video output stage of the

Functional Description (Continued)

LM1269, giving a high impedance at the output pin. After bits 0 and 1 of register 9 are set to a 1, the power supplies to the CRT driver and CRT can be turned off.

Note: The 5V supply must remain on for proper operation. Since the LM1269 is a CMOS device its power consumption will be minimal.

External DACs: Four DACs with external outputs are provided in the LM1269. Normally these DACs will be used for color balance and brightness control. If the brightness control is done at G1, then three DACs would be used for color balance and the last DAC would be used for controlling the G1 voltage.

There is also a provision to set the brightness at the cathodes. DAC 4 can be set to vary the outputs of the other three DACs after the color balance is completed. This is accomplished by adding the output of DAC 4 to the other 3 DACs. Bits 3 and 4 of register 9 are set to a 1 for brightness control at the cathodes. Bit 3 sets the output range of DAC 1–3 to 50% of their full range. Bit 4 adds 50% of DAC 4 to the other three DACs. These two adjustments keeps the overall output voltage of DAC 1–3 in the proper range and still allows brightness control. For either mode of brightness control, the DACs are ideally set to work with the LM2479 or LM2480 for DC restoration at the cathodes of the CRT.

ESD and Arc-Over Protection

The LM1269 incorporates full ESD protection with special consideration given to maximizing arc-over robustness. The monitor designer must still use good circuit design and PCB layout techniques. The human body model ESD susceptibility of the LM1269 is 3.5 kV, however many monitor manufacturers are now testing their monitors to the level 4 of the IEC 801-2 specification which requires the monitor to survive an 8 kV discharge. External ESD protection is needed to survive this level of ESD. The LM1269 provides excellent protection against both ESD and arc-over, but this is not a substitute for good PCB layout.

Figure 7 shows the recommended input protection for the LM1269. This provides the best protection against ESD. When this protection is combined with good PCB layout the LM1269 will easily survive the IEC 801-2 level 4 testing (8 kV ESD). It is strongly recommended that the protection diodes be added as shown in *Figure 7*. The 1N4148 diode has a maximum capacitance of 4 pF, which will have little effect on the response of the video system due to the low impedance of the input video.

The ESD cells of the LM1269 also provide good protection against arc-over, however good PCB layout is necessary. The LM1269 should not be exposed directly to the voltages that may occur during arc-over. The main vulnerability of the LM1269 to arc-over is though the ground traces on the PCB. For proper protection all ground connections associated with the LM1269, including the grounds to the bypass capacitors, must have short returns to the ground pins. A significant ground plane should be used to connect all the LM1269 grounds. *Figure 10*, which shows the demo board layout, is an excellent example of an effective ground plane. The list below should be followed to ensure a PCB with good grounding:

- All grounds associated with the LM1269 should be connected together through a large ground plane.
- CRT driver ground is connected to the video pre-amp ground at one point.
- CRT and arc protection grounds are connected directly to the chassis or main ground. There is no arc-over current flow from these grounds through the LM1269 grounds.
- Input signal traces for SDA, SCL, H Flyback, and Clamp should be kept away from the CRT driver and all traces that could carry the arc current.
- Output signal traces of the LM1269 should be kept away from the traces that carry the output signals of the CRT driver.

If any one of the above suggestions is not followed the LM1269 may become more vulnerable to arc-over. Improper grounding is by far the most common cause of video pre-amp failure during arc-over.

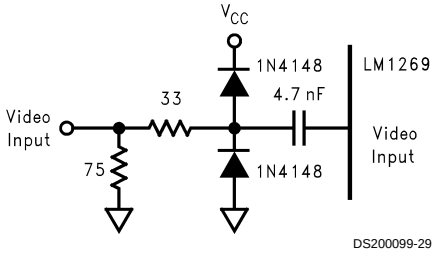


FIGURE 7. Recommended Video Input ESD Protection

Schematic

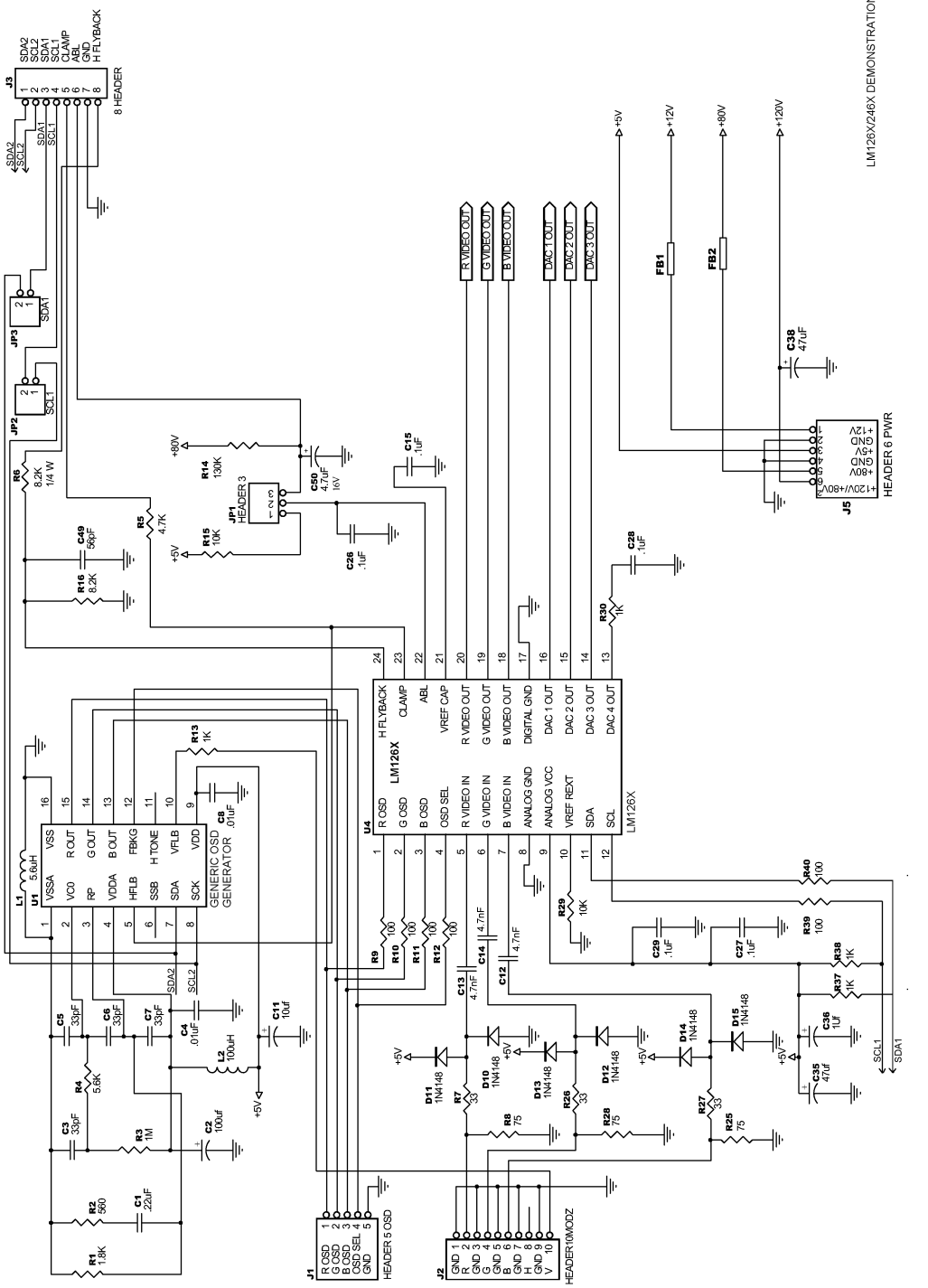


FIGURE 8. LM126X/LM246X Neck Board Schematic

Schematic (Continued)

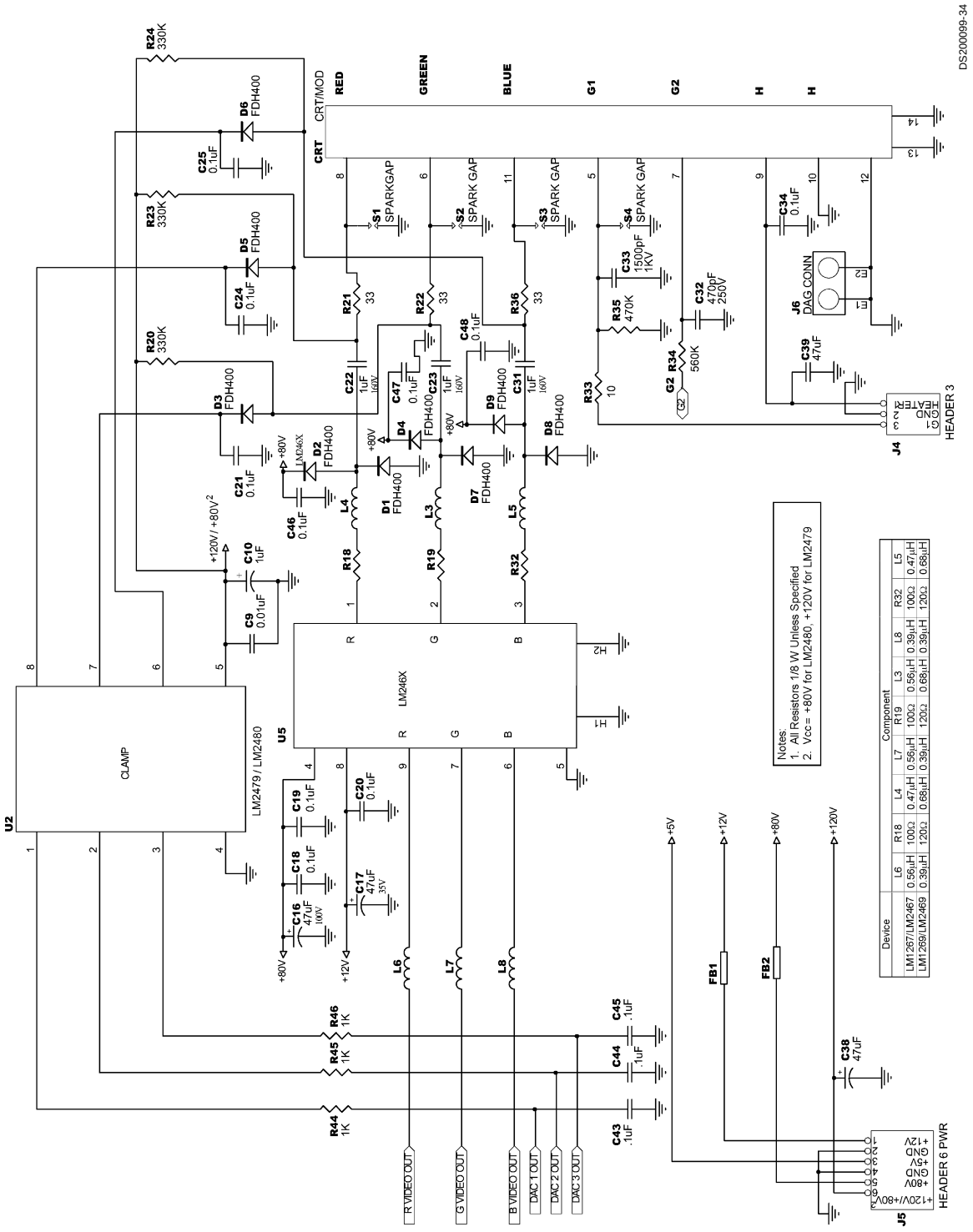


FIGURE 9. LM126X/LM246X Neck Board Schematic (Continued)

PCB Layout

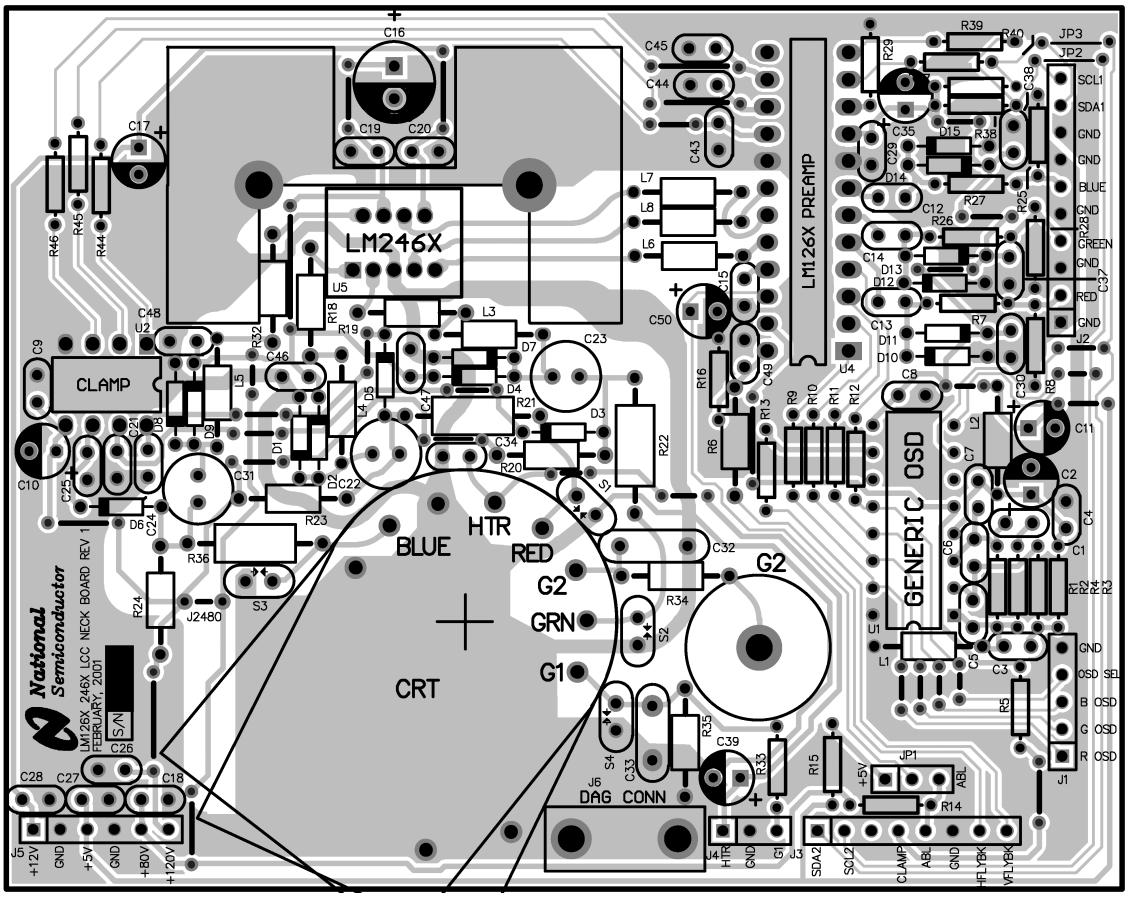


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FIGURE 10. LM126X/LM246X System Neck Board

Micro-Controller Interface

The micro-controller interfaces to the LM1269 pre-amp via an I^2C interface. The protocol of the interface begins with the Start Pulse followed by a byte comprised of a seven-bit Slave Device Address and a Read/Write bit as the LSB. Therefore the address of the LM1269 for writing is DCh (1101 1100) and the address for reading is DDh (1101 1101). *Figures 11, 12* show a write and read sequence across the I^2C interface.

Write Sequence

The write sequence begins with a start condition which consists of the master pulling SDA low while SCL is held high. The slave device address is next sent. The address byte is made up of an address of seven bits (7–1) and the read/write bit (0). Bit 0 is low to indicate a write operation. Each byte that is sent is followed by an acknowledge. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The address of the register to be written to is sent next. Following the register address and the acknowledge bit the data for the register is sent. If bit 0 of register 0Ah is set low (default value) then the LM1269 is set for the increment mode. In this mode when more than one data byte is sent it is automatically incremented into the next address location. See *Figure 11*. Note that each data byte is followed by an acknowledge bit.

Read Sequence

Read sequences are comprised of two I^2C transfer sequences. The first is a write sequence that only transfers the address to be accessed. The second is a read sequence that starts at the address transferred in the previous address write access and incrementing to the next address upon every data byte read. This is shown in *Figure 12*.

The write sequence consists of the Start Pulse, the Slave Device Address including the Read/Write bit (a zero, indicating a write), then its Acknowledge bit. The next byte is the address to be accessed, followed by its Acknowledge bit and the stop bit indicating the end of the address only write access.

Next the read data access is performed beginning with the Start Pulse, the Slave Device Address including the Read/Write bit (a one, indicating a read) and the Acknowledge bit. The next 8 bits will be the data read from the address indicated by the write sequence. Subsequent read data bytes will correspond to the next increment address locations. Each data byte is separated from the other data bytes by an Acknowledge bit.

Micro-Controller Interface (Continued)

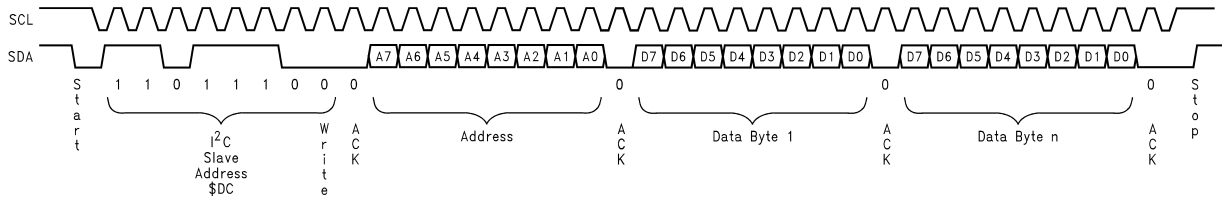


FIGURE 11. I²C Write Sequence

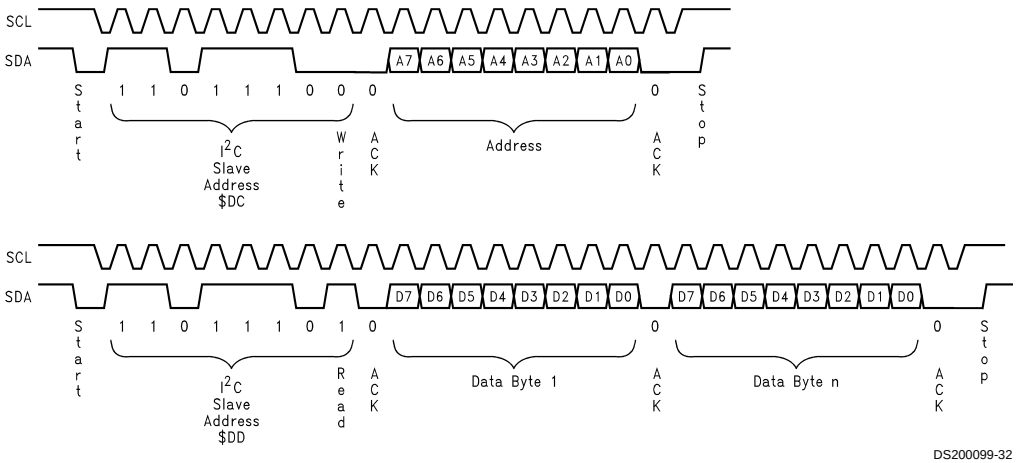


FIGURE 12. I²C Read Sequence

I²C Interface Registers

I²C IC ADDRESS

Slave Address of the LM1269 is DCh when writing to the registers and DD when reading from the registers.

LM1269 Pre-Amp Interface Registers (all numbers in Hex)

Register	Address	Default	Format							
R Gain Control	00	60h	X	R Gain [6:0]						
B Gain Control	01	60h	X	B Gain [6:0]						
G Gain Control	02	60h	X	G Gain [6:0]						
Contrast Cont.	03	60h	X	Contrast [6:0]						
DAC1	04	80h	DAC 1[7:0]							
DAC2	05	80h	DAC 2[7:0]							
DAC3	06	80h	DAC 3[7:0]							
DAC4	07	80h	DAC 4[7:0]							
DC Offset/ OSD Cont.	08	15h	X	X	X	OSD_Cont. [1:0]		DC_Offset [2:0]		
Global Control	09	00h	X	X	O	DCF4	DCF1–3	O	PS	BV
Increment Mode	0A	00h	X	X	X	X	X	X	O	INCR
Software Reset	0F	00h	X	X	X	X	X	X	X	SRST

Pre-Amp Interface Registers

Red Channel Gain Control Register (I²C address 00h)

Register name: R Gain Control (00h)

Bit 7							Bit 0
RSV	RG6	RG5	RG4	RG3	RG2	RG1	RG0

Bits 6–0: Red Channel Gain Control. These seven bits determine the gain for the Red Channel.

Bit 7: Reserved.

Blue Channel Gain Control Register (I²C address 01h)

Register name: B Gain Control (01h)

Bit 7							Bit 0
RSV	BG6	BG5	BG4	BG3	BG2	BG1	BG0

Bits 6–0: Blue Channel Gain Control. These seven bits determine the gain for the Blue Channel.

Bit 7: Reserved.

Green Channel Gain Control Register (I²C address 02h)

Register name: G Gain Control (02h)

Bit 7							Bit 0
RSV	GG6	GG5	GG4	GG3	GG2	GG1	GG0

Bits 6–0: Green Channel Gain Control. These seven bits determine the gain for the Green Channel.

Bit 7: Reserved.

Contrast Control Register (I²C address 03h)

Register name: Contrast Control (03h)

Bit 7							Bit 0
RSV	CG6	CG5	CG4	CG3	CG2	CG1	CG0

Bits 6–0: Contrast Control. These seven bits vary the gain of all three channels.

Bit 7: Reserved.

DAC Interface Register Definitions

DAC 1 Register (I²C address 04h)

Register name: DAC 1 (04h)

Bit 7							Bit 0
D1–7	D1–6	D1–5	D1–4	D1–3	D1–2	D1–1	D1–0

Bits 7–0: DAC 1. These eight bits determine the output voltage of DAC 1.

DAC 2 Register (I²C address 05h)

Register name: DAC 2 (05h)

Bit 7							Bit 0
D2–7	D2–6	D2–5	D2–4	D2–3	D2–2	D2–1	D2–0

Bits 7–0: DAC 2. These eight bits determine the output voltage of DAC 2.

DAC 3 Register (I²C address 06h)

Register name: DAC 3 (06h)

DAC Interface Register Definitions

(Continued)

Bit 7							Bit 0
D3–7	D3–6	D3–5	D3–4	D3–3	D3–2	D3–1	D3–0

Bits 7–0: DAC 3. These eight bits determine the output voltage of DAC 3.

DAC 4 Register (I^2C address 07h)

Register name: DAC 4 (07h)

Bit 7							Bit 0
D4–7	D4–6	D4–5	D4–4	D4–3	D4–2	D4–1	D4–0

Bits 7–0: DAC 4. These eight bits determine the output voltage of DAC 4.

DC Offset and OSD Contrast Control Register (I^2C address 08h)

Register name: DC Offset/OSD Cont. (08h)

Bit 7							Bit 0
RSV	RSV	RSV	OSDC1	OSDC0	DC2	DC1	DC0

Bits 2–0: DC Offset Control. These three bits determine the active video DC offset to all three channels.

Bits 4–3: OSD Contrast Control. These two bits determine the contrast level of the OSD information.

Bits 7–5: Reserved.

Global Video Control Register (I^2C address 09h)

Register name: Global Control (09h)

Bit 7							Bit 0
RSV	RSV	0	DCF4	DCF1–3	0	PS	BV

Bit 0: Blank Video. When this bit is a one, blank the video output. When this bit is a zero allow normal video out.

Bit 1: Power Save. When this bit is a one, shut down the analog circuits to support sleep mode. When this bit is a zero enable the analog circuits for normal operation.

Bit 2: MUST BE SET TO "0" FOR PROPER OPERATION.

Bit 3: DAC1–3 Configuration. When this bit is a zero the DAC outputs of DAC1–3 are full scale (0V–4.5V). When this bit is 1, the range of DAC1–3 are halved (0V–2.25V).

Bit 4: DAC4 Configuration. When this bit is a zero the DAC4 output is not mixed with the other DAC outputs. When the bit is one, 50% of the DAC4 output is added to DAC1–3.

Bit 5: MUST BE SET TO "0" FOR PROPER OPERATION.

Bits 7–6: Reserved.

Increment Mode Register (I^2C address 0Ah)

Register name: Increment Mode (0Ah)

Bit 7							Bit 0
RSV	RSV	RSV	RSV	RSV	RSV	TST	INCR

Bit 0: Increment Enable. When set to a "0", the default value, the increment mode is enabled. This allows the registers to be updated sequentially by sending another block of data.

Bit 1: MUST BE SET TO "0" FOR PROPER OPERATION.

Bits 7–2: Reserved.

Software Reset Register (I^2C address 0Fh)

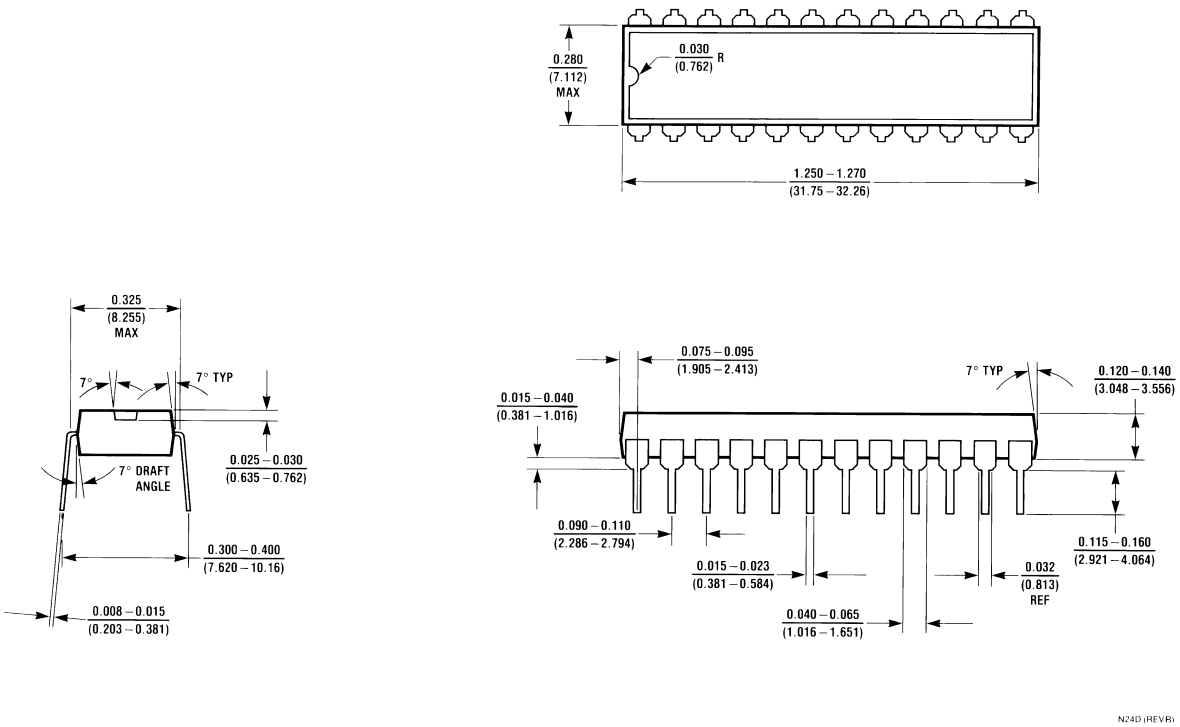
Register name: Software Reset (0Fh)

Bit 7							Bit 0
RSV	RSV	RSV	RSV	RSV	RSV	RSV	SRST

Bit 0: Software Reset. Setting this bit causes a software reset. All registers (except this one) are loaded with their default values. All operations currently in progress are aborted (except for I^2C transactions). This bit automatically clears itself when the reset has been completed.

Bits 7–1: Reserved.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM1269NA
NS Package Number N24D

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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